Oxide Reliability of SiC MOSFETs

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Personal Information

- Georgia State University - Physics B.S.
- Entering 4th year of studies
- Previous research on:
  - Biophysics – FTIR Spectroscopy
  - Optoelectronics – Infrared / UV photodetectors
- Graduate studies in Engineering
Outline

- Background: Transistor (MOSFET), Silicon Carbide (SiC)
- Drain Current ($I_D$) and Threshold Voltage ($V_{TH}$) Instability
- Experimental Setup
- Results: $I_D$ and $V_{TH}$ Instability at different temperatures
- Conclusions
MOSFET Basics

- Metal Oxide Semiconductor Field Effect Transistor
- Functions as electronic switch in integrated circuits (ICs)
- E-fields accumulate charge carriers
- Create a conductive channel
SiC Background: Advantages

- Physical Characteristics:
  - Wide $E_{\text{gap}}$ (3.26 eV)
  - High thermal conductivity (x2 Si)
  - High saturated drift velocity (higher than GaAs)
  - Radiation hard
  - Native oxide

- Useful Applications:
  - High temperature electronics
  - High power electronics
  - Space
SiC Applications
SiC Background: Drawbacks

- Low mobility (10 cm² / V s)
- $V_{TH}$ instability which causes current degradation

In this work:

- Study temperature dependence of $I_D$ and $V_{TH}$ instability
$V_{TH} = 2\Phi_F + \Phi_{MS} - \frac{\sqrt{4q_0\varepsilon Si N_A \Phi_F}}{C_{ox}} \left( \frac{Q_{ox}}{C_{ox}} \right)$

$I_D = \frac{W}{L} \mu_{eff} C_{OX} \left[ (V_G - V_{TH}) V_D - \frac{1}{2} V_D^2 \right]$

oxide charge causes $V_{TH}$ Shift

$I_D$ and $V_{TH}$ Instability in MOSFETs
Experimental Setup

T = 77K – 400K

B1500A Parameter Analyzer

Fast IV Set Up

Cryogenic Probe Station
Results: DC Measurements (slow)

- $I_D$ decreases substantially as temperature is lowered
- $V_{TH}$ increases as we decrease temperature
- This rise is attributed to an increased amount of trapped carriers in the oxide at lower temperatures
Results: Mobility Extraction

- Mobility decreases as temperature was reduced
- Coloumbic scattering is the dominant mechanism
- It is suggested that filled traps at the interface could be the cause for the scattering
Physical Model I: Fermi Potential Increase

- Fermi potential increases with decreasing temperature
- As a result, more traps are filled at threshold
- The increased oxide charge increases $V_{TH}$ and scattering
Results: Fast IV Measurements

- $V_{TH}$ relaxation does not occur since measurement times were short (10 μs)
- $I_D$ decreases while $V_{TH}$ increases as temperature is lowered
Results: Pulse Response
(Fast and Slow Measurement)

- Fast measurements agree with DC measurements results
- The degradation is larger and faster as temperature decreases
Conclusions

- The performance of SiC MOSFETs depends greatly on temperature.
- As the temperature is lowered, $V_{TH}$ increases, while mobility and $I_D$ decrease.
- This thermally activated process is attributed to change in traps occupation in the oxide.
Conclusion – cont.

- This is good news for high temperature and high power application
- Low temperature applications will require a substantial reduction of the interface traps density
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Questions ?